



香港中文大學

The Chinese University of Hong Kong

*CENG3430 Rapid Prototyping of Digital Systems*  
**Lecture 00: Course Information**

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[mcyang@cse.cuhk.edu.hk](mailto:mcyang@cse.cuhk.edu.hk)



# CENG3430 Course Information



- **CENG3430 Rapid Prototyping of Digital Systems**
- **Course Time and Place**
  - **Lecture (\*2)**
    - MON 12:30~14:15 (@[LSB LT2](#))
  - **Lab (\*2)**
    - TUE 14:30~16:15 (@SHB 102)
    - **Required to attend both lab sessions**
- **Course Website**
  - <http://www.cse.cuhk.edu.hk/~mcyang/ceng3430/2223T2/ceng3430.html>
  - <https://blackboard.cuhk.edu.hk/>

# Course Instructor & Teaching Assistants

- **Course Instructor**

- Prof. Ming-Chang YANG (楊明昌)

- Office: SHB 906
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- **Teaching Assistants**

- Lok Yin CHOW (周樂言)

- Office: SHB 921
- Email: [lychow@cse.cuhk.edu.hk](mailto:lychow@cse.cuhk.edu.hk)



- Zelin DU (杜澤林)

- Office: SHB 921
- Email: [zldu22@cse.cuhk.edu.hk](mailto:zldu22@cse.cuhk.edu.hk)



# We are surrounded by digital systems!

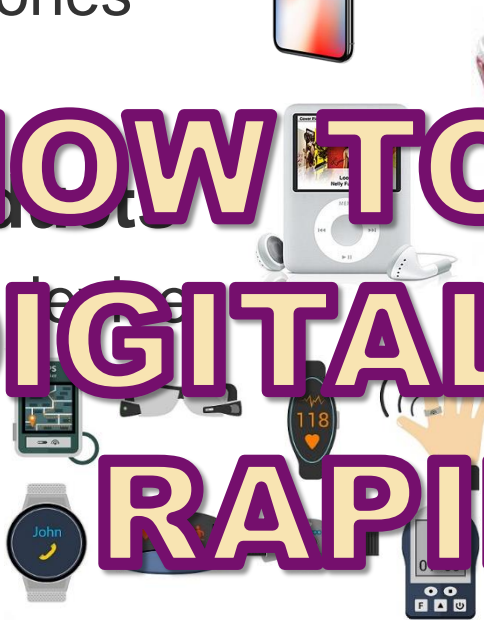
- **Mass Products**

- Media players
- Mobile phones



- **Novel Products**

- Wearable devices
- Robots

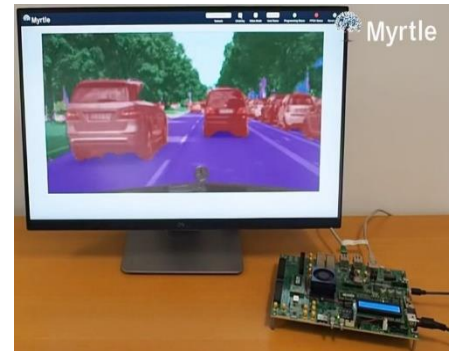


## HOW TO BUILD A DIGITAL SYSTEM RAPIDLY?



- **Research**

- Real time edge detection
- Deep learning acceleration



# Common Design Flow of Digital System



Idea Generation

Drafting on Paper

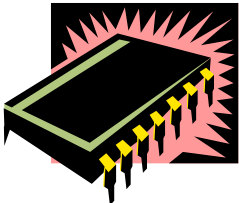
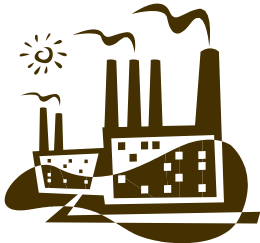
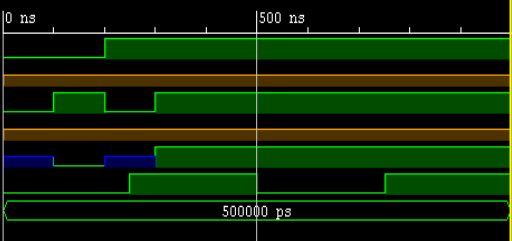
Designing Chip (HDL)

Testing (FPGA)

Manufacturing  
Production Line Design

Quality Control

```
Ex: VHDL AND-Gate Program
1 entity and2 is
2 port (a,b: in std_logic;
3       c: out std_logic);
4 end and2
5 architecture arch of and2
6 begin
7     c <= a and b;
8 end and2_arch
```



# Our Focus: Prototyping



Idea Generation

Drafting on Paper

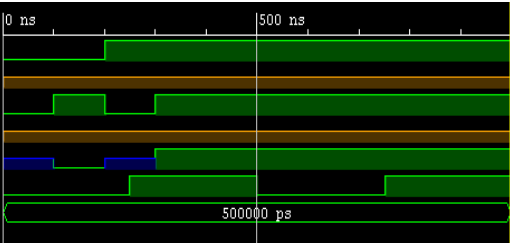
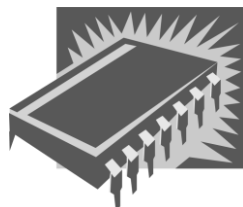
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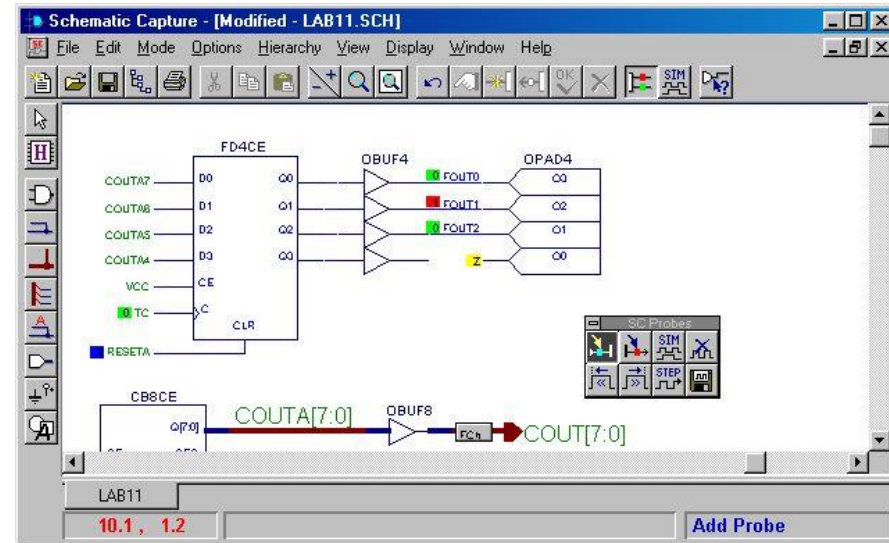
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```



# Methods for Digital System Design



- **Schematic Method**
  - **Complicated**
  - Suitable for **top level design** to merge **modules**
    - Like data flow block diagram



- **Programming Language**

- **VHDL** (Very-High-Speed-Integrated-Circuits Hardware Description Language)
  - Each **module** in the schematic can be implemented by VHDL.
- **Verilog**

```
Ex: VHDL AND-Gate Program  
1 entity and2 is  
2 port (a,b: in std_logic;  
3       c: out std_logic);  
4 end and2  
5 architecture and2_arch of and2  
6 begin  
7     c <= a and b;  
8 end and2_arch
```

# What We Will Learn: HDL + FPGA

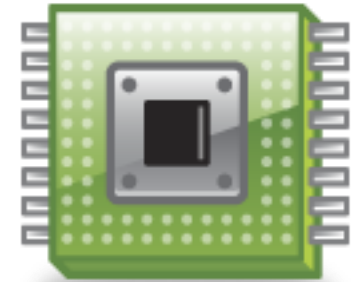


- **Software:** Hardware Description Language (HDL)

**Ex: VHDL AND-Gate Program**

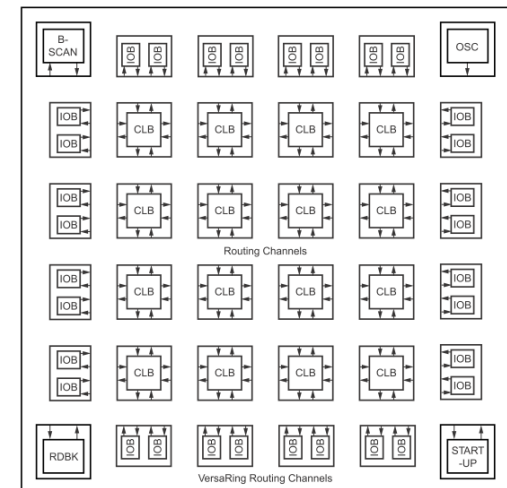
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3       c: out std_logic);
4 end and2
5 architecture and2_arch of and2
6 begin
7     c <= a and b;
8 end and2_arch
```

*Write HDL code,  
then it will generate  
the hardware chip  
automatically*



- **Hardware:** Field Programmable Gate Array (FPGA)

- The hardware can be **reprogrammable**.
- Designs can be changed **easily**.
- No additional hardware manufacturing **cost** is needed.

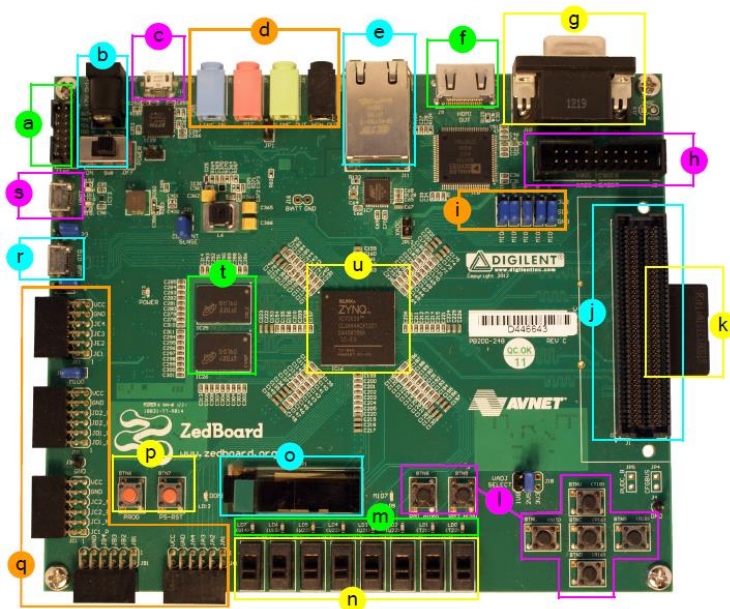




# What We Will Use



- **Software:** Vivado WebPACK™ Edition (**FREE**)
  - It supports **Windows** or **Linux** operating systems.
  - **Hardware Description Language:** Very-High-Speed-Integrated-Circuits Hardware Description Language (**VHDL**)
- **Hardware:** Zynq ZedBoard
  - Dual-core ARM Cortex-A9 with traditional FPGA



- |                                 |                                |                                    |
|---------------------------------|--------------------------------|------------------------------------|
| <b>a</b> Xilinx JTAG connector  | <b>h</b> XADC header port      | <b>o</b> OLED display              |
| <b>b</b> Power input and switch | <b>i</b> Configuration jumpers | <b>p</b> Prog & reset push buttons |
| <b>c</b> USB-JTAG (programming) | <b>j</b> FMC connector         | <b>q</b> 5 x Pmod connector ports  |
| <b>d</b> Audio ports            | <b>k</b> SD card (underside)   | <b>r</b> USB-OTG peripheral port   |
| <b>e</b> Ethernet port          | <b>l</b> User push buttons     | <b>s</b> USB-UART port             |
| <b>f</b> HDMI port (output)     | <b>m</b> LEDs                  | <b>t</b> DDR3 memory               |
| <b>g</b> VGA port               | <b>n</b> Switches              | <b>u</b> Zynq device (+ heatsink)  |

# Software: Vivado WebPACK™ Edition



example - [E:/example/example.xpr] - Vivado 2016.3

File Edit Flow Tools Window Layout View Help

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design
- Program and Debug
  - Bitstream Settings
  - Generate Bitstream
  - Open Hardware Manager

Project Manager example

Sources

Messages: 1 warning

- Design Sources (1)
  - example - example\_arch (example.vhd)
- Constraints
- Simulation Sources (1)

Hierarchy Libraries Compile Order

Source File Properties

example.vhd

Enabled

Location: E:/example/example.srcs/sources\_1/new

Type: VHDL

Library: xil\_defaultlib

Size: 0.6 KB

General Properties

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	PCIe %	Start	Elapsed	Strateg
synth_1	constrs_1	Not started															Vivado
impl_1	constrs_1	Not started															Vivado

Tcl Console Messages Log Reports Design Runs

Project Summary example.vhd

Project Settings

Project name: example

Project location: E:/example

Product family: Zynq-7000

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1)

Top module name: example

Target language: VHDL

Simulator language: Mixed

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit

Board part name: em.avnet.com.zed.part01.3

Repository path: C:/Xilinx/Vivado/2016.3/data/boards/board\_files

URL: <http://www.zedboard.org>

Board overview: ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status: Not started

Messages: No errors or warnings

Implementation

Status: Not started

Messages: No errors or warnings

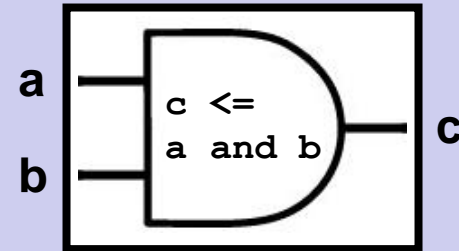
# Hardware Description Language: VHDL

- **An Example: AND-Gate in VHDL**

## Entity Declaration: Define I/Os

```
1 entity and2 is
2   port (a,b: in std_logic;
3         c: out std_logic);
4 end and2
```

```
5 architecture and2_arch of and2
6 begin
7   c <= a and b;
8 end and2_arch
```

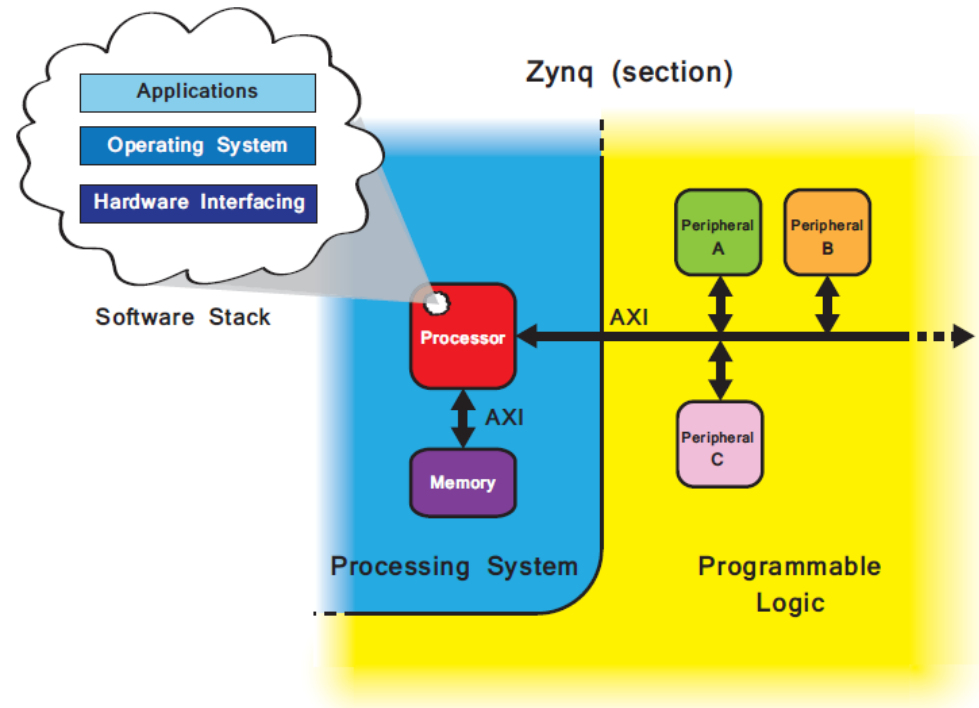
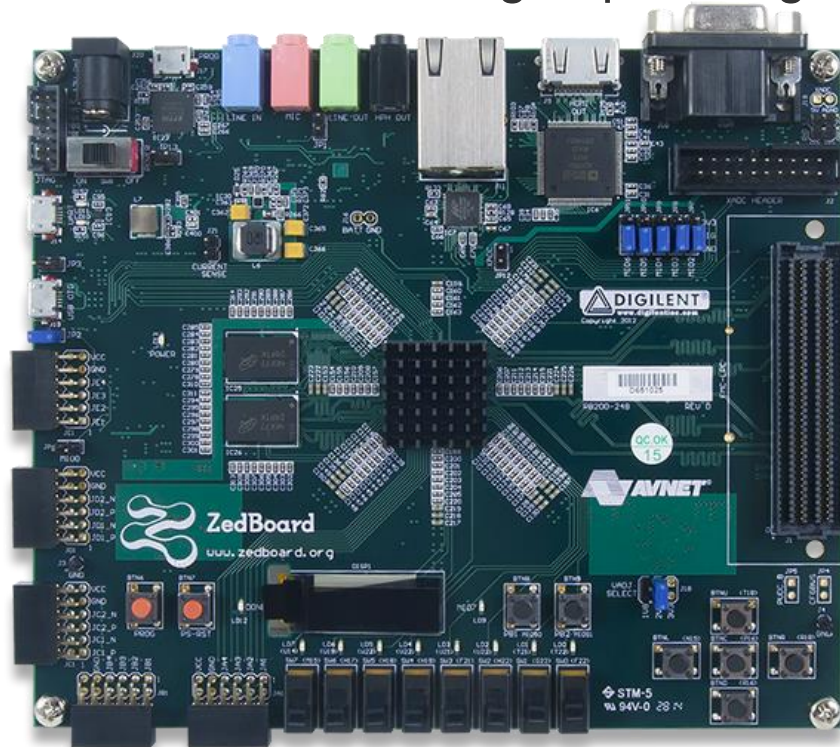


## Architecture Body: Define functions

# Hardware: Zynq ZedBoard



- Zynq ZedBoard combines
  - **Processing System (PS):** Dual-core ARM Cortex-A9 CPU
    - Supports software routines and/or operating systems
  - **Programmable Logical (PL):** Equivalent to trad. FPGA
    - Ideal for high-speed logic, arithmetic and data flow subsystems



# Course Assessment



- **Grading** (*subject to changes*)
  - Class Participation 10%
    - Unable to attend? Raise **leave requests** via email
  - Weekly Lab Exercises 40%
    - Required to submit **individually**
  - Final Project 50%
    - **At most two** students in a group
  - Bonus up to 5% (be active!)
- **Note**
  - Late submission is **NOT** acceptable (unless otherwise approved before the regular deadline).

# Class Participation? uReply




1) Enter the  
**Session Number**

2) Confirm the  
**Session Number**  
and Click **“Join”**

3) Login with  
**Student ID** and  
**CWEM Password**

Language English



Session Number (Required)


Student ID (Optional)

Student name (Optional)

Remember my student ID and student name

JOIN


Language English



LC5376

CWEM login after 'join'

JOIN



**CWEM Authentication**

This session requires your CWEM account.

LC5376

1155123456

.....|

JOIN

## [uReply Attendance User Guide](#)

# Recordings? Panopto Video



- 2022R2 Rapid Prototyping of Digital Systems (CENG3430)
- Notifications
- Announcements
- Course Contents
- Discussion Board
- Groups
- My Grades
- Library
- Reading List
- Panopto Video**

## Panopto Content

搜索在目錄中"2022R2-CENG3430: 2022R2 Rapid Pro" + 創建 由Panopto技術支援 ?

2022R2-CENG3430: 2022R2 Rapid Prototyping of Digital S... ? + 訂閱 ?

排序 :: 名稱 持續時間 日期 ▼ 評級

Lab Recordings Lecture Recordings 新增影片庫

# Course Schedule (tentative)






W	Date	Lecture	Lab
1	Jan. 9, 10	Lec00: Course Information	No Lab (for the first week)
2	Jan. 16, 17	Lec01: Introduction to VHDL	Lab01: Vivado & Software Simulation
3	Jan. 23, 24	Lunar New Year Vacation (No Class)	Lunar New Year Vacation (No Lab)
4	Jan. 30, 31	Lec02: Introduction to ZedBoard	Lab02: First Program on ZedBoard
5	Feb. 6, 7	Lec03: Comb. Circuit and Seq. Circuit	Lab03: Shift Register
6	Feb. 13, 14	Lec04: Finite State Machine	Lab04: Finite State Machine
7	Feb. 20, 21	Lec05: Driving VGA Display	Lab05: Driving VGA Display
8	Feb. 27, 28	Lec06: Driving Peripheral Modules	Lab06: Driving Peripheral Modules
9	Mar. 6, 7	Reading Week (No Class)	Public Holiday (No Lab)
10	Mar. 13, 14	Lec07: Integration of ARM and FPGA	Lab07: Software Stopwatch
11	Mar. 20, 21	Lec08: Embedded Operating System	Lab08: Software Stopwatch with Linux
12	Mar. 27, 28	Lec09: High Level Synthesis	Lab09: High Level Synthesis Exercise
13	Apr. 3, 4	Final Project Proposal	Final Project Proposal
14	Apr. 10, 11	Public Holiday – Easter (No Class)	Feedback on Final Project Proposal
15	Apr. 17, 18	Lec10: VHDL versus Verilog	Lab10: Verilog Exercise
	TBD	Final Project Final Submission (Demo Video and Report) Deadline	





# Full Final Project List (2021-22)



1. [Hit to Dance](#)
2. [Digital Companion Pet](#) 
3. [Wordle](#)
4. [Pixel Space Invader](#)
5. [CUHKO](#)
6. [Smart Home Device](#)
7. [Breakout Clone](#)
8. [Vending Machine](#) 
9. [Mario with ZedBoard](#)
10. [Vending Machine](#)
11. [Color Vision Game](#)
12. [Vending Machine](#)
13. [Math Game](#)
14. [Mirrored Snake](#)
15. [Audio Recording & Playback](#)
16. [Don't Stop Photon](#)
17. [Color Memory Game](#)
18. [T-Rex Runner](#)
19. [Sliding Puzzle Game](#)
20. [Health Monitoring Cell](#)
21. [Snack Game](#)
22. [Duck Hunt](#) 
23. [Sliding Game](#)
24. [FPonGA](#)
25. Le Cheers

# Full Final Project List (2020-21)



1. Digital Locker 
2. Weather Report Generation 
3. Reaction Game
4. Snake Game
5. Audition (Rhythm Game)
6. Kernel Convolution
7. GOMOKU
8. Football Shooting Game
9. Catch the Thief
10. The Snake Game
11. FLAPPY BIRD
12. Mota Game
13. Flappy Bird
14. Snake Game



WOW IDEA

# Full Final Project List (2019-20)





1. AVG Game
2. Door Locking System
3. The Flappy Bird 🏆
4. Immigration System
5. Traffic Horn Punishment
6. How Fast Is Your Finger
7. Mastermind
8. Drum Looper
9. Gobang
10. Morse Code from Torch
11. Indoor Monitoring Station
12. Rhythm Game
13. Cat Dog Fight Game
14. Portable Freezer 🏆
15. Color Detector
16. Mastermind
17. Tic Tac Toe
18. UFO Catcher
19. Sound Recorder



WOW IDEA

# Full Final Project List (2018-19)



1. [Piano and Music Player](#)
2. [Color Recognition](#)
3. [RGB Meter](#)
4. [Lie Detector](#) 
5. [Snake Battle](#)
6. [Space War](#)
7. [The Dodge Game](#)
8. [Space Impact](#)
9. [Get It at Once](#)
10. [Elevator](#) 
11. [Super Pads](#)
12. [Tetris](#)
13. [Morse Code Interpreter](#)
14. [The Flash](#)
15. [Multifunctional Display](#)
16. [Rolling Down!](#)

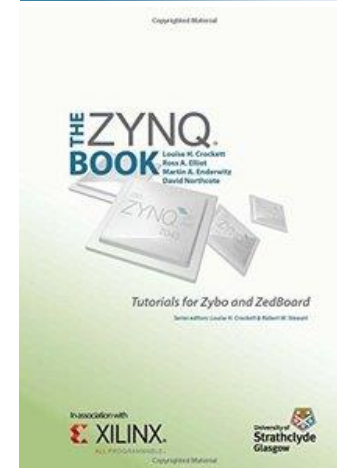
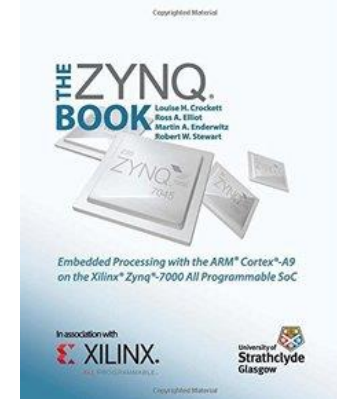
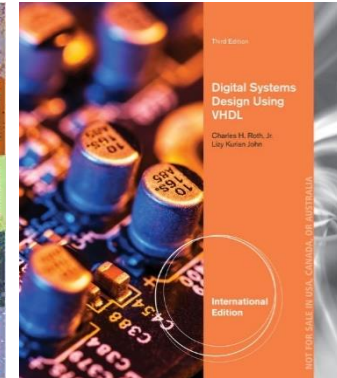
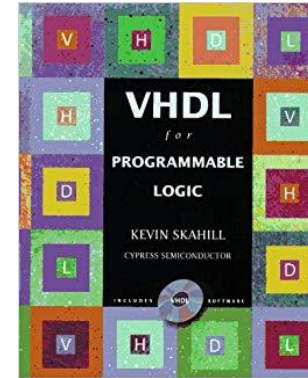


WOW IDEA

# References



- **VHDL for Programmable Logic**
  - Kevin Skahill
  - Addison-Wesley
- **Digital Systems Design Using VHDL**
  - Charles H. Roth Jr., Lizy Kurian John
  - Cengage Learning
- **The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc**
  - Louise H Crockett, Ross A Elliot, Martin A Enderwitz, Robert W Stewart
  - Strathclyde Academic Media
- **The Zynq Book: Tutorials for Zybo and ZedBoard**
  - Louise H Crockett, Ross A Elliot, Martin A Enderwitz
  - Strathclyde Academic Media



# Important Notes



- Visit our course website regularly!
- Plagiarism will **NOT** be tolerated!
  - Don't copy!
  - Don't let other(s) copy!
  - Can discuss but write up the solutions by yourself!
- Honesty in Academic Work:
  - <http://www.cuhk.edu.hk/policy/academichonesty/>

*The best way to learn is through practice!*

# Severe Penalties on Dishonesty (1/3)

(iii)	<p><b>Employing or using services</b> provided by a third party [Note 1] to undertake the examinations/ final year projects/ papers/ essays/ dissertations, or providing services as a third party, including any one of the following aspects:</p> <p>(a) employing or using services provided by a third party;</p> <p>(b) providing services as a third party;</p> <p>(c). sharing of any materials obtained from the employment or use of services provided by a third party to other students; and</p> <p>(d) knowingly using materials obtained by anyone who has employed or used the services provided by a third party.</p>	(i)	three demerits (of which one will remain in the University's record permanently and two are reviewable);
		(ii)	a failure grade for the course concerned (not applicable to the student who is the third party to provide the services but not taking the same course or not taking it in the same term);
		(iii)	<b>suspension from the University</b> for one term [Note 2]; and
		(iv)	<b>lowering the degree classification</b> by one level upon graduation (not applicable to undergraduate students who graduate with a Pass Degree, MBChB students and postgraduate students) [Note 3].
(v)	<p><b>Distribution/ Sharing/ Copying</b> of teaching materials without the consent of the course teachers to gain unfair academic advantage in the courses</p>	(i)	two demerits.

# Severe Penalties on Dishonesty (2/3)

(vi)	<p>Violating rule 15 or 16 of the University's Examination Rules (<a href="#">Annex 1</a>) or rule 9 or 10 of the University's Online Examination Rules (<a href="#">Annex 2</a>)</p>	<p><u>First offence</u></p> <p>(i) one demerit.</p> <p><u>Second or further offence (and a first offence that is serious as decided by the disciplinary committee concerned/the FTP Committee)</u></p> <p>(i) two demerits (of which one will remain in the University's record permanently and one is reviewable).</p>
(vii)	<p>Cheating in tests and examinations (including violation of rule 17 or 18 of the University's Examination Rules or rule 11, 12, 13, 14 or 16 of the University's Online Examination Rules)</p>	<p><u>First offence</u></p> <p>(i) one demerit (which will remain in the University's record permanently); and</p> <p>(ii) a failure grade for the course concerned.</p> <p><u>Second or further offence (and a first offence that is serious as decided by the disciplinary committee concerned/the FTP Committee)</u></p> <p>(i) two demerits (of which one will remain in the University's record permanently and one is reviewable); and</p> <p>(ii) a failure grade for the course concerned.</p>



# Severe Penalties on Dishonesty (3/3)

(viii)	Impersonation fraud in tests and examinations (including violation of rule 19 of the University's Examination Rules or rule 15 of the University's Online Examination Rules)	(i)	three demerits (of which one will remain in the University's record permanently and two are reviewable);
		(ii)	a failure grade for the course concerned;
		(iii)	suspension from the University for one term [Note 1]; and
		(iv)	lowering the degree classification by one level upon graduation (not applicable to undergraduate students who graduate with a Pass Degree, MBChB students and postgraduate students) [Note 2].
		[The same penalties apply to the student who asks/allows someone to assume his/her identity to sit for a test/an examination as well as to the student who sits for a test/an examination if both parties are students of the University, except that penalty (ii) will not apply to the latter.]	